R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 4 lines 21-28, page 6 lines 25-30, page 7 lines 10-14, page 7 lines 27-32, page 9 lines 11-13 and FIGS. 3, 5 and 6, as originally filed, and claim 26. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-5, 7-10, 15, 16, 18, 19, 21 and 23-26 under 35 U.S.C. §103(a) as being unpatentable over O'Connor '667 in view of Yonemitsu et al '840 (hereafter Yonemitsu) has been obviated by appropriate amendment and thus should be withdrawn.

The rejection of claim 11 under 35 U.S.C. §103(a) as being unpatentable over O'Connor and Yonemitsu in further view of Russo '383 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 14, 20, 22 and 27 under 35 U.S.C. §103(a) as being unpatentable over O'Connor has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

O'Connor concerns a method of time shifting to simultaneously record and play a data stream (Title). Yonemitsu concerns methods and devices for encoding and decoding frame signals and recording medium therefore (Title). Russo concerns a video time-shifting apparatus (Title). In contrast, claim 1 provides (in part) steps for (i) a first buffering of an input signal having a digital video format and (ii) compressing the input signal substantially simultaneously with the buffering, the compressing including (iii) a second buffering of the input signal. Assuming, *arguendo*, that it may have been obvious to store data in a buffer memory 18 of Yonemitsu substantially simultaneously to compressing an input signal (for which Applicants' representative does not necessarily agree), the combination of O'Connor and Yonemitsu still appears to be silent regarding two buffering steps for the input signal. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest steps for (i) a first buffering of an input signal having a digital video format and (ii) compressing the input signal substantially simultaneously with the buffering, the compressing including (iii) a second buffering of the input signal as presently claimed.

Claim 1 further provides a step for delivering a plurality of real-time video frames along a first processing path to an output for display in response to the input signal as first buffered. In contrast, the proposed combination of O'Connor and

Yonemitsu appears to be silent regarding a bypass 142 of O'Connor (asserted similar to the first processing path) carrying an input signal **as buffered by the buffer memory 18 of Yonemitsu** (asserted similar to the first buffering). Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest a step for delivering a plurality of real-time video frames along a first processing path to an output for display in response to the input signal as first buffered as presently claimed. As such, claim 1 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 20 provides a real-time decoder configured to generate a first output signal by decompressing a compressed digital video input signal. In contrast, the video in 102 block of O'Connor (asserted similar to the claimed real-time decoder) does not appear to have a decompression capability. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest a real-time decoder configured to generate a first output signal by decompressing a compressed digital video input signal as presently claimed.

Furthermore, the Office Action provides no evidence of motivation to modify O'Connor. In particular, no evidence is provided why one of ordinary skill in the art would combine the video out unit 120 of O'Connor and the video in unit 102 of O'Connor into a single unit similar to the claimed real-time decoder. Therefore, *prima facie* obviousness has not been

established. As such, claim 20 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 21 provides a controller separate from an encoder and a time-shifted decoder and configured to (i) receive a first intermediate signal and (ii) present a second intermediate signal and a frame storage system directly connected to the controller and configured to generate the second intermediate signal. In contrast, each of O'Connor and Yonemitsu appear to be silent regarding intermediate signals flowing through a controller to and from a frame storage system. Therefore, O'Connor and Yonemitsu do not teach or suggest a controller separate from an encoder and a time-shifted decoder and configured to (i) receive a first intermediate signal and (ii) present a second intermediate signal and a frame storage system directly connected to the controller and configured to generate the second intermediate signal as presently claimed.

Claim 21 further comprises a time-shifted decoder separate from the controller and configured to generate a second output signal by decompressing the second intermediate signal (presented by the controller). In contrast, both O'Connor and Yonemitsu appear to be silent regarding a decoder receiving an intermediate signal from a controller. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest a time-shifted decoder separate from the controller and configured to generate a second output signal by decompressing the second

intermediate signal as presently claimed. As such, claim 21 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 22 provides a real-time decoder configured to generate a first output signal in response to decompressing a video input signal. Despite the assertion on page 11 of the Office Action, the video in 102 unit of O'Connor does not appear to have a decompression capability. Therefore, O'Connor does not teach or suggest a real-time decoder configured to generate a first output signal in response to decompressing a video input signal as presently claimed.

Furthermore, the Office Action provides no evidence of motivation to modify O'Connor. In particular, no evidence is provided why one of ordinary skill in the art would combine the video out unit 120 of O'Connor and the video in unit 102 into a single unit similar to the claimed real-time decoder. Therefore, *prima facie* obviousness has not been established. As such, claim 22 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 23 provides a first frame buffer configured to (i) generate a first signal and a second signal by buffering an input signal, (ii) pause the first signal at a frame during a transition from a real-time mode to a time-shifted mode and (iii) buffer a third signal. In contrast, each of O'Connor and Yonemitsu appear to be silent regarding a frame buffer capable of generating two

signals from one buffered signal, buffer two different signals and pause one of the signals. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest a first frame buffer configured to (i) generate a first signal and a second signal by buffering an input signal, (ii) pause the first signal at a frame during a transition from a real-time mode to a time-shifted mode and (iii) buffer a third signal as presently claimed.

Claim 23 further provides (i) an encoder connected to the first frame buffer and configured to generate the third signal by compressing the second signal and (ii) a controller connected to the first frame buffer to receive the third signal. In contrast, each of O'Connor and Yonemitsu appear to be silent regarding an encoder receiving a second signal from a buffer and compressing the second signal to generate a third signal that is stored back into the frame buffer. Therefore, O'Connor and Yonemitsu, alone of in combination, do not teach or suggest (i) an encoder connected to a first frame buffer and configured to generate a third signal by compressing a second signal and (ii) a controller connected to the first frame buffer to receive the third signal as presently claimed.

Claim 23 further provides (i) the controller connected to the first frame buffer to receive the third signal and (ii) a buffer connected to the controller to store the third signal. In contrast, each of O'Connor and Yonemitsu appear to be silent regarding a buffer storing a signal received from a frame buffer

through a controller. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest (i) a controller connected to a first frame buffer to receive a third signal and (ii) a buffer connected to the controller to store the third signal as presently claimed. As such, claim 23 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 4 provides a transition from a real-time mode to a time-shifted mode is triggered by a single command of a viewer. In contrast, O'Connor appears to contemplate two user commands to transition between modes. For example, FIG. 7 of O'Connor illustrates a first user input 702 to transition from a real-time to a paused condition and a second user input 706 to transition from the paused to a time-delayed condition. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest a transition from a real-time mode to a time-shifted mode is triggered by a single command of a viewer as presently claimed. As such, claim 4 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 8 provides that real-time video frames are provided from a decoder that decompresses an input signal. The assertion on page 5 of the Office Action that a decoder is inherent to decompressing compressed video appears to be satisfied by the decompression unit 110 of O'Connor. However, the decompression unit 110 of O'Connor provides time-shifted frames, not real-time frames as presently claimed. Furthermore, O'Connor does not appear

to teach that both the bypass option and the reception of compressed video option may be implemented simultaneously. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest that real-time video frames are provided from a decoder that decompresses an input signal as presently claimed. As such, claim 8 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 11 provides that the transition is from a particular real-time video frame to a next frame (in display sequence after the particular real-time video frame) of time-shifted video frames. In contrast, each of O'Connor, Yonemitsu and Russo appear to be silent regarding a transition from one frame from the real-time frames to a subsequent frame from the time-shifted frames. Therefore, O'Connor, Yonemitsu and Russo, alone or in combination, do not teach or suggest a transition from a particular real-time video frame to a next frame of time-shifted video frames as presently claimed. As such, claim 11 is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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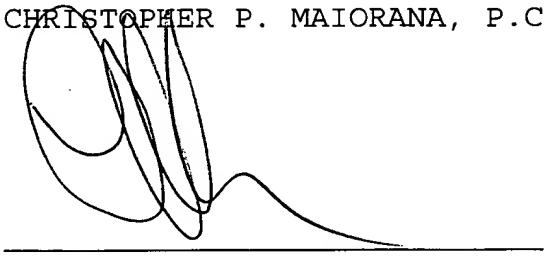

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